IN THE CLAIMS

We claim:

1. A method of forming a doped source region comprising:

forming a dielectric filled trench isolation region in a silicon substrate, said dielectric filled trench isolation region isolating a first portion of said silicon substrate from a second portion of said silicon substrate;

removing a portion of said dielectric in said trench to reveal a portion of said silicon substrate in said trench between said first and said second portions of said silicon substrate; and

implanting ions to form a first doped source region in said first portion of said silicon substrate, to form a second doped source region in said second portion of the said silicon substrate and to form a doped region in said revealed silicon substrate in said trench, said doped region in said trench extending from said first doped source region to said second doped source region.

2. The method of 5 wherein said dielectric film trench isolation regions have sidewalls tapered at an angle between 80 – 60° from the surface of said silicon substrate.

3. The method of 5 wherein ions are implanted perpendicular to the surface of said silicon substrate.

4. A method of forming a flash memory integrated circuit comprising:

forming a trench in a silicon substrate;

growing an oxide in said trench;

removing said grown oxide from said trench;

growing a second oxide in said trench;

filling said trench with a dielectric;

growing a tunnel oxide on said silicon substrate adjacent to said dielectric filled trench;

forming a first polysilicon layer on said tunnel oxide;

forming an interpoly dielectric on said first polysilicon layer;

forming a polysilicon control gate on said interpoly dielectric.

5. A method of forming a flash memory integrated circuit comprising:

forming a first and a second polysilicon/dielectric/polysilicon stack on a tunnel oxide of a substrate, wherein said first and second stacks are separated by a gap;

forming a shared source region in said gap between said first and said second polysilicon/dielectric/polysilicon stacks;

forming a first drain region adjacent to said first stack on the side opposite said shared source region;

forming a second drain region adjacent to said second stack on the side opposite said shared source region;

forming a dielectric layer over said first and said second stacks and over said first and said second drains wherein said dielectric layer completely fills said gap between said first and second stacks;

antisotropically etching said dielectric layer from said first drain region and said second drain region so as to form a first spacer on the side of said first stack adjacent to said first drain and to form a second spacer on the side of said second stack adjacent to said second drain wherein in after said antisotropic etch steps said gap remains filled with said dielectric.

6. A method of forming a flash memory integrated circuit comprising:

forming a tunnel oxide on a substrate;

forming and patterning a first polysilicon film on said tunnel oxide;

forming a interpoly dielectric on said patterned first polysilicon film;

forming a second polysilicon film over said interpoly dielectric over said first patterned polysilicon film;

polishing said second polysilicon film to form a second polysilicon film with a substantially planar top surface; and

etching said second polysilicon film, said interpoly dielectric, and said planarized second polysilicon film to form a polysilicon/dielectric/polysilicon stack having a planar top surface.

7. A method of forming a flash memory integrated circuit comprising:

forming a first and a second polysilicon/dielectric/polysilicon stacks on a tunnel oxide formed on a silicon substrate, said first and said second stacks separated by a gap;

forming a shared source region in said silicon substrate in said gap and a first drain region adjacent to said first stack opposite said shared source region, and a second drain region adjacent to said second stack opposite said shared source;

forming a dielectric layer over said first drain over said first stack over said shared source, over said second stack, and over said second drain;

antisotropically etching said dielectric to form spacer on said first drain adjacent to said first stack and a second spacer on said second drain adjacent to said second stack;

forming a metal film over said first drain, said first spacer, said first stack, said second stack, said second spacer, and said second drain; and

heating said substrate to cause said metal to react with said silicon in said first and said second drain regions and with said polysilicon of said first and second stacks to form a metal silicide on said first drain, said second drain, and on said top polysilicon of said first and second stacks.